

FIG. 1

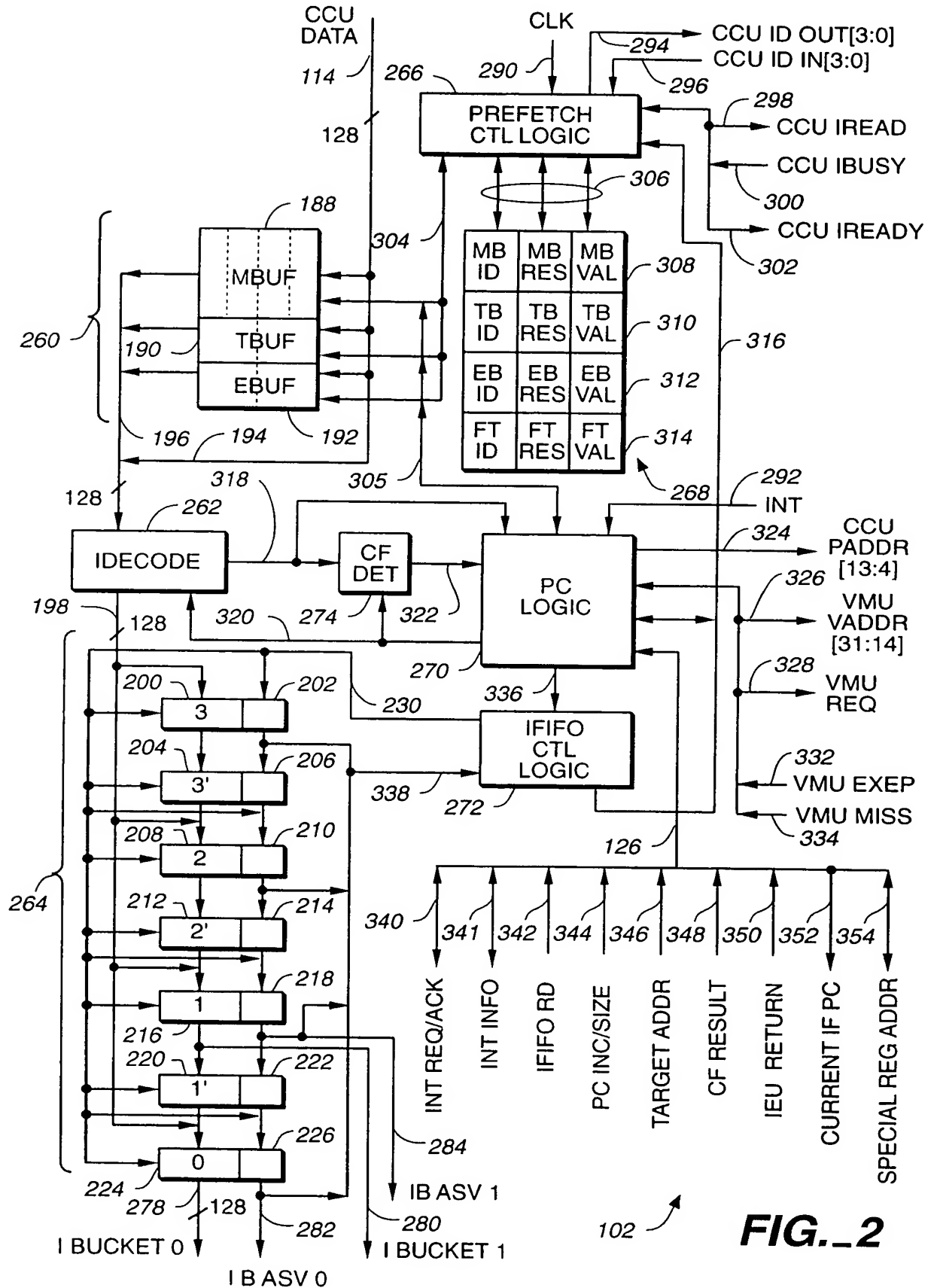


FIG. 2

FIG. 3 is a block diagram of a PC control system, designated by reference numeral 270. The system includes three main control units: a PREFETCH PC CONTROL UNIT, an EXECUTION PC CONTROL UNIT, and a PFPC CTL INC (Prefetch PC Control Unit Incrementer). An INT CONTROL UNIT (Interrupt Control Unit) is also shown at the bottom right.

Input/Output Signals:

- Inputs to PREFETCH PC CONTROL UNIT:** CCU PADDR (324), VMU VMADDR (326), and VMU VADDR (326).
- Inputs to EXECUTION PC CONTROL UNIT:** OPERAND DISPLACEMENT (352'), PFPC (364), and REL (382).
- Inputs to PFPC CTL INC:** VMU VADDR (326), VMU REQ (328), and CF DETECT (322).
- Inputs to INT CONTROL UNIT:** INT REQ/ACK (340), NMI (292), IRQ (292), LVL (292), VM MISS (334), VM EXEP (332), and INT INFO (341).

Internal Signals and Connections:

- PFPC CTL INC:** Outputs PC CONTROL UNIT (372), Ex PC CTL (378), INC/SIZE (380), and INT. OFFSET (373).
- PREFETCH PC CONTROL UNIT:** Outputs PFPC (364) to the EXECUTION PC CONTROL UNIT and RETURN ADDR (382) to the EXECUTION PC CONTROL UNIT.
- EXECUTION PC CONTROL UNIT:** Outputs ABS (346) to the INT CONTROL UNIT and TARGET ADDR (354) to the INT CONTROL UNIT.
- INT CONTROL UNIT:** Outputs SUSPEND PREFETCH (343) to the PFPC CTL INC and INT REQ/ACK (340) to the INT CONTROL UNIT.
- Other Signals:** CF/IDECODE CTL (320), IEU RETURN (350), CF RESULT (348), PC INC/SIZE (344), and IFIFO RD (342) are also shown as signals within the system.

FIG. 3

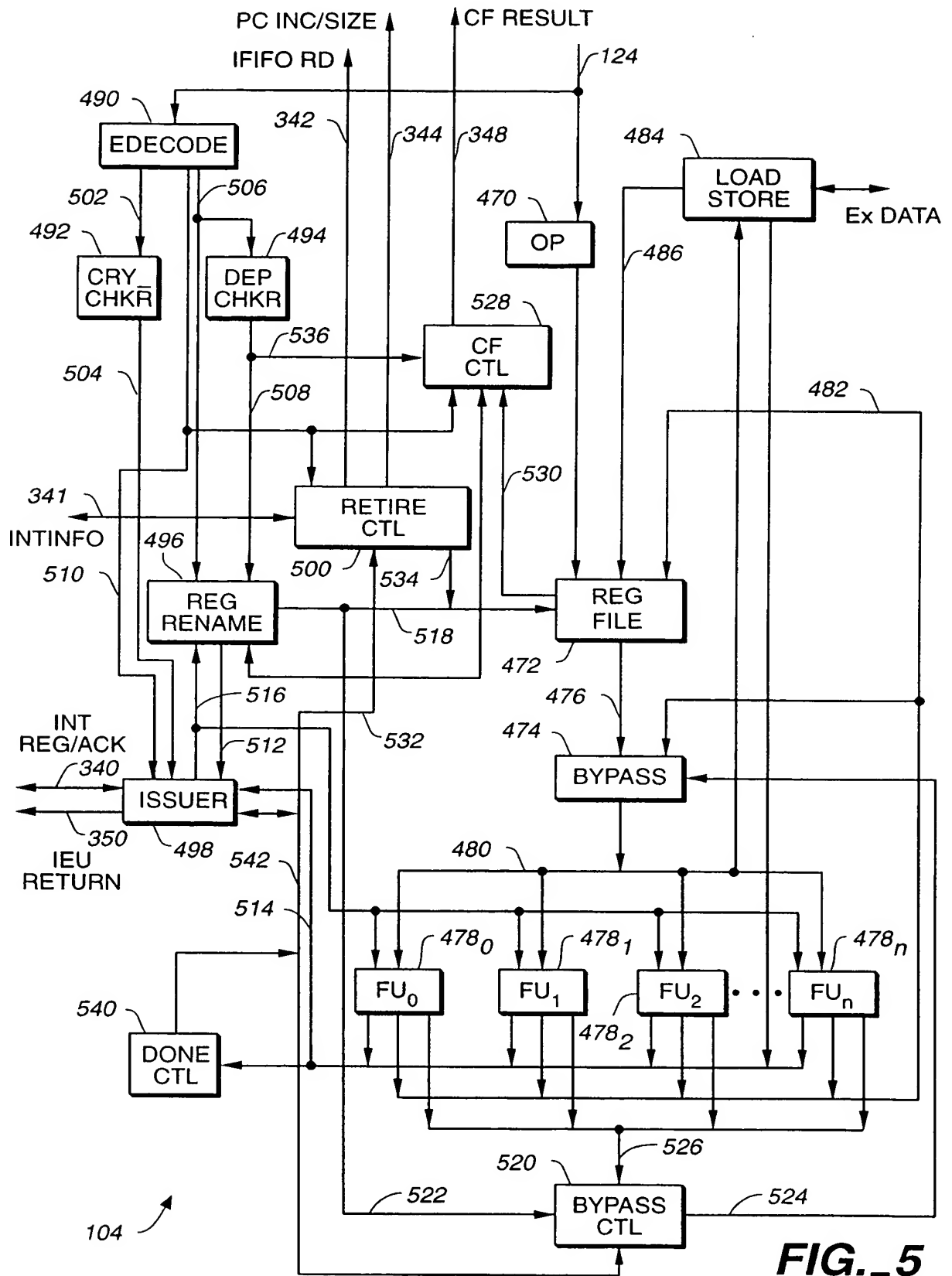


FIG. 5

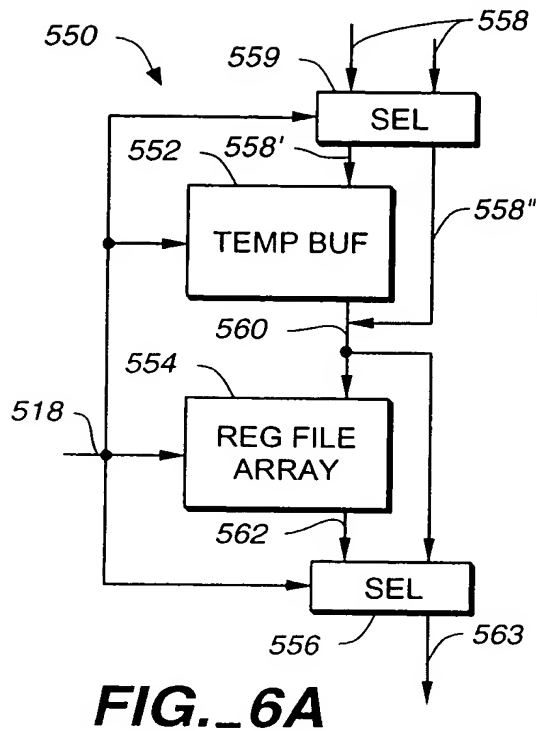


FIG. 6A

TEMP BUF

I3RD	I7RD
I2RD	I6RD
I1RD	I5RD
I0RD	I4RD

FIG. 6B

I7	I6	I5	I4
I3	I2	I1	I0

FIG. 6C

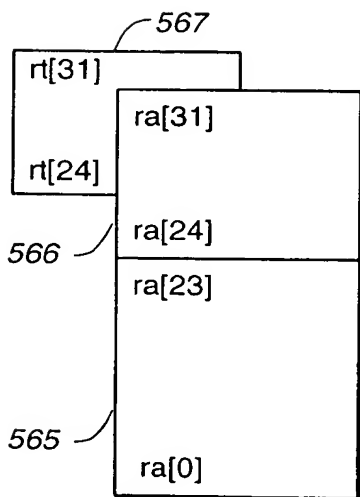


FIG. 7A

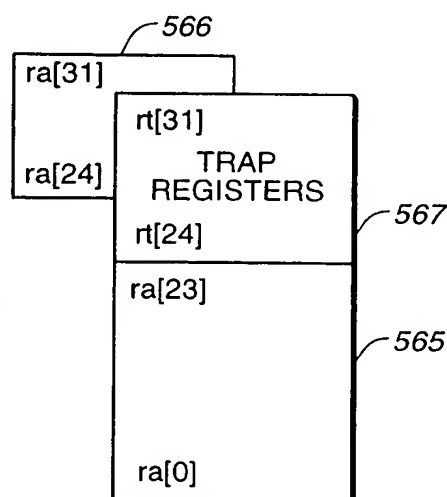


FIG. 7B

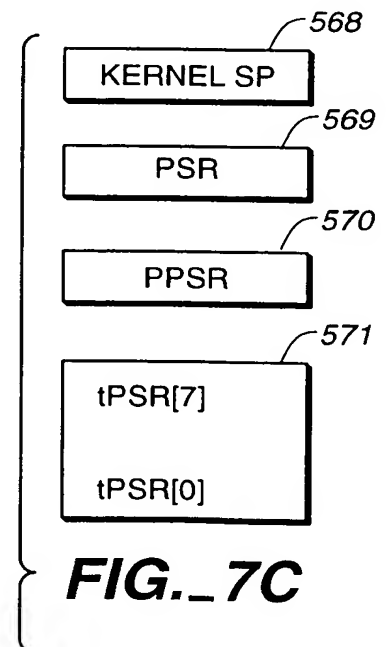


FIG. 7C

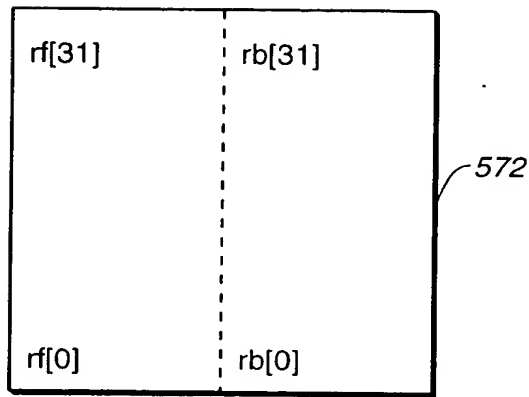


FIG. 8

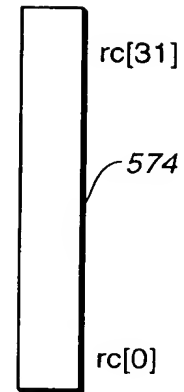


FIG. 9

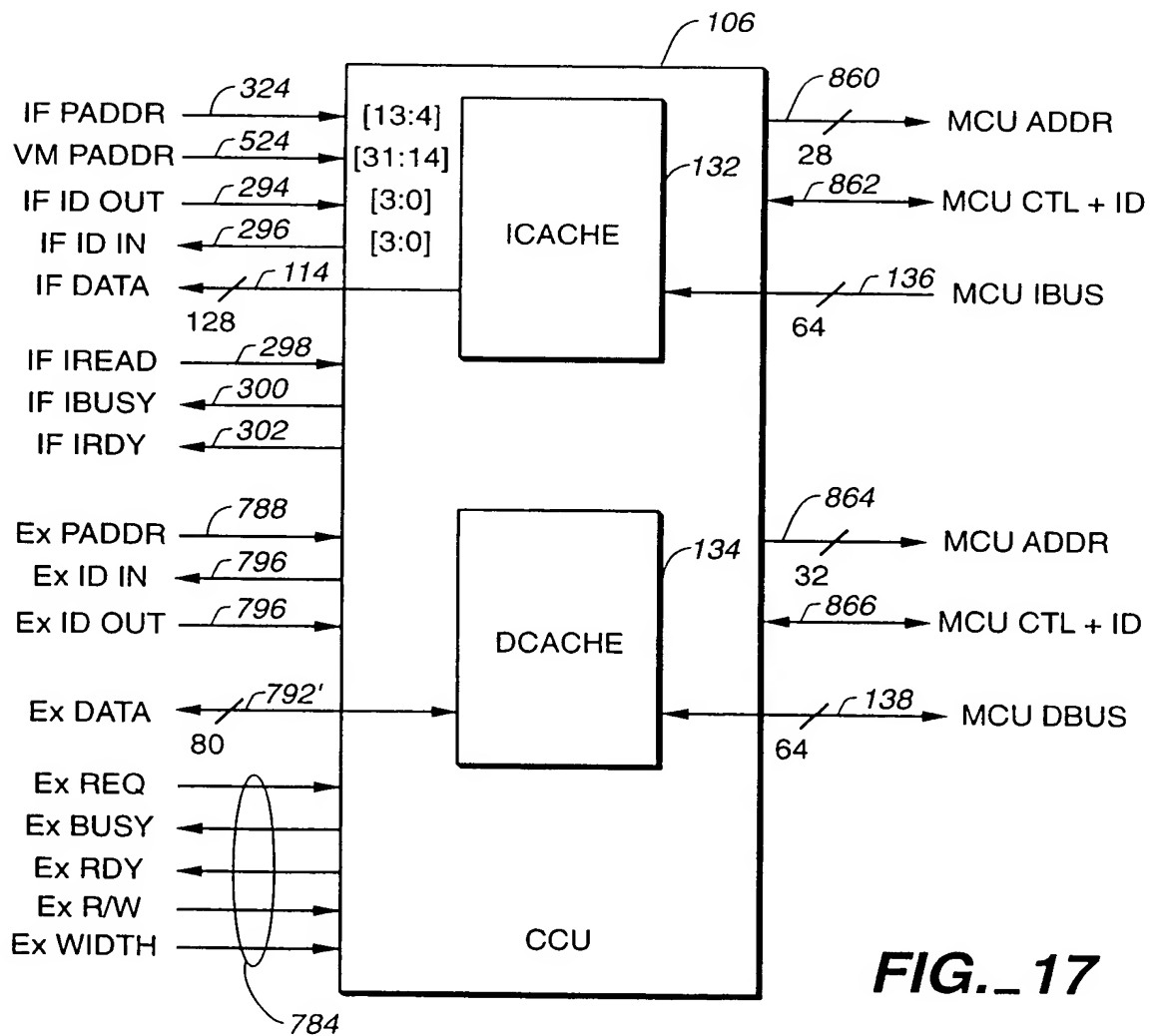


FIG. 17

FIG. 10

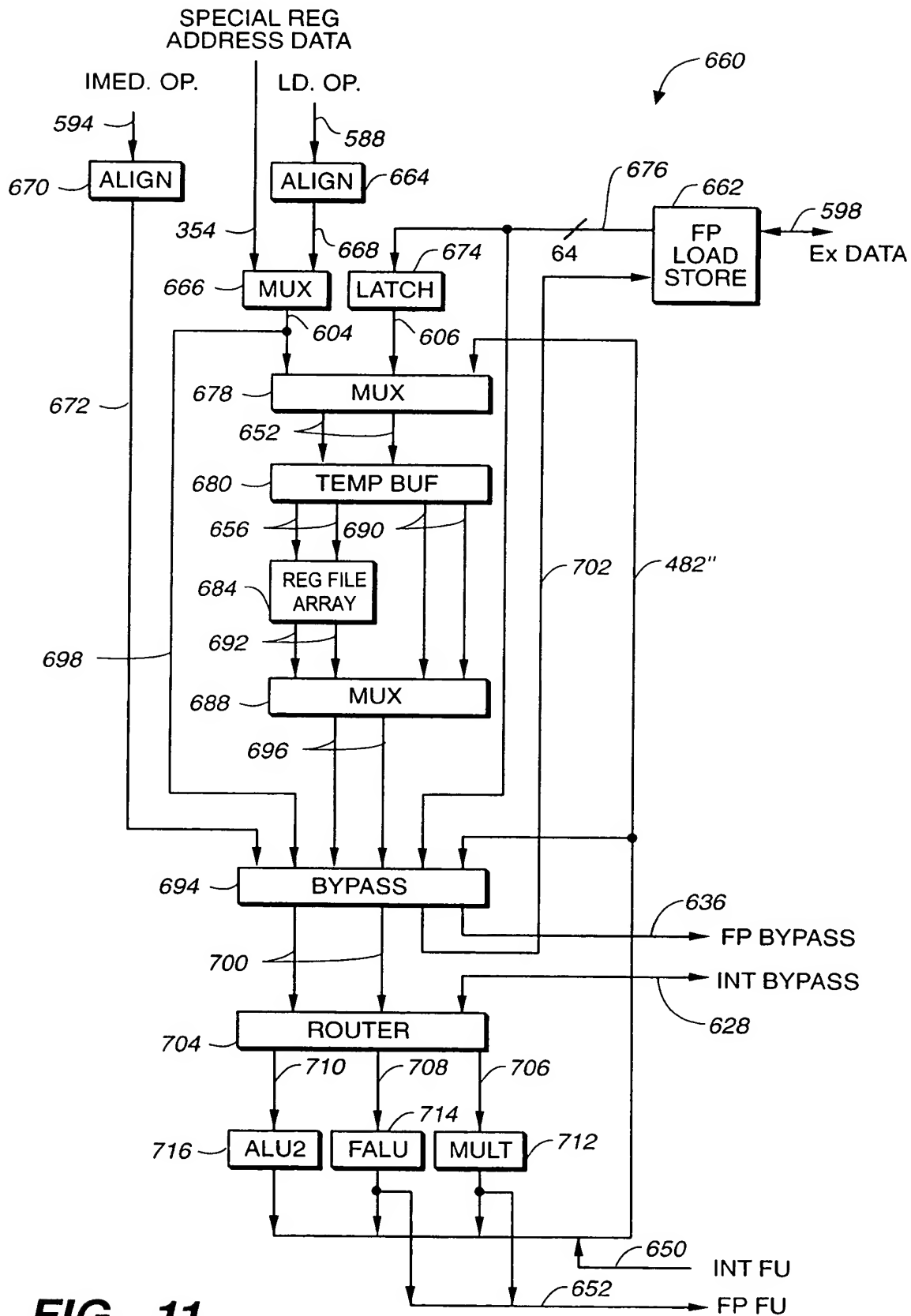


FIG. 11

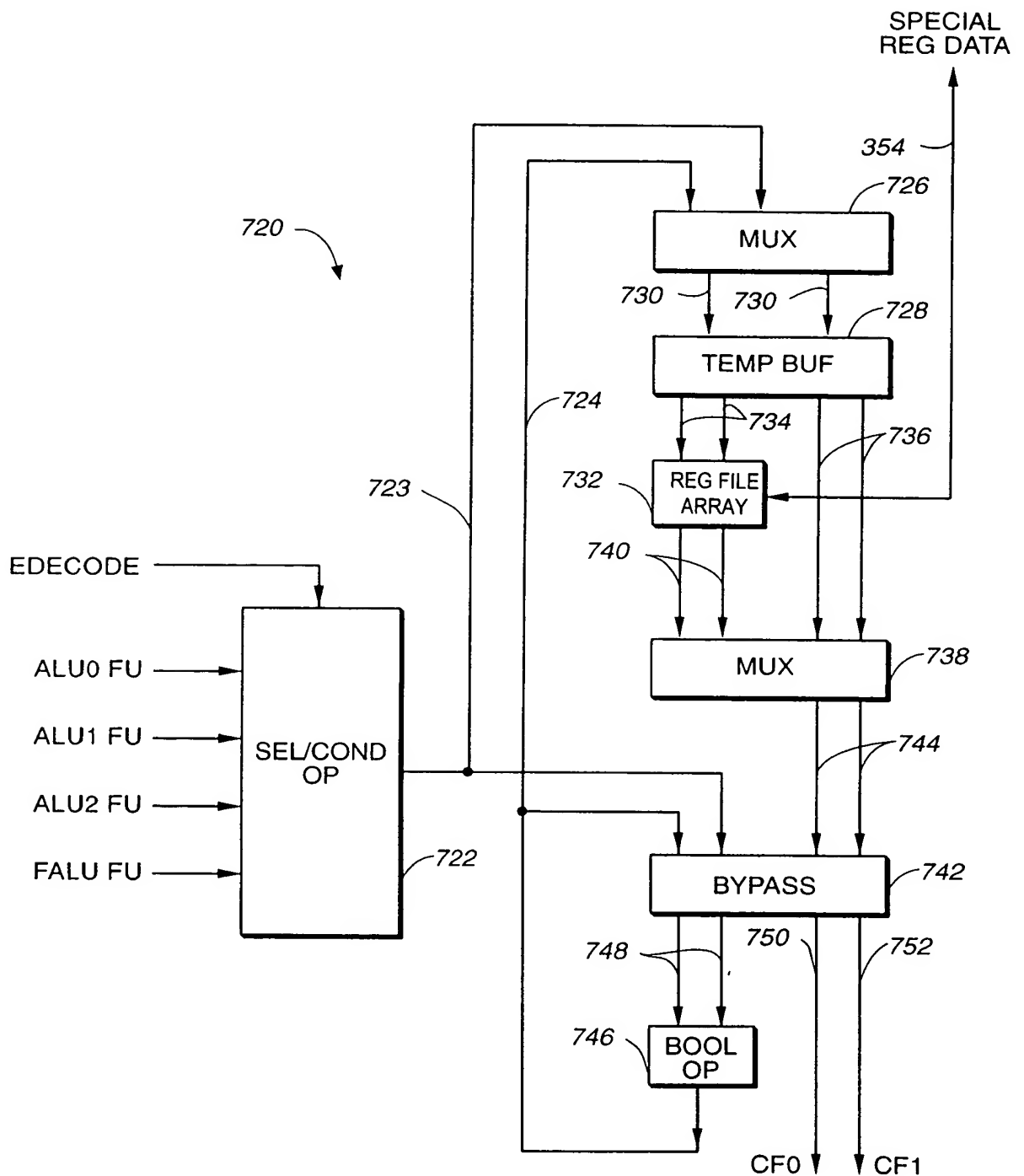


FIG. 12

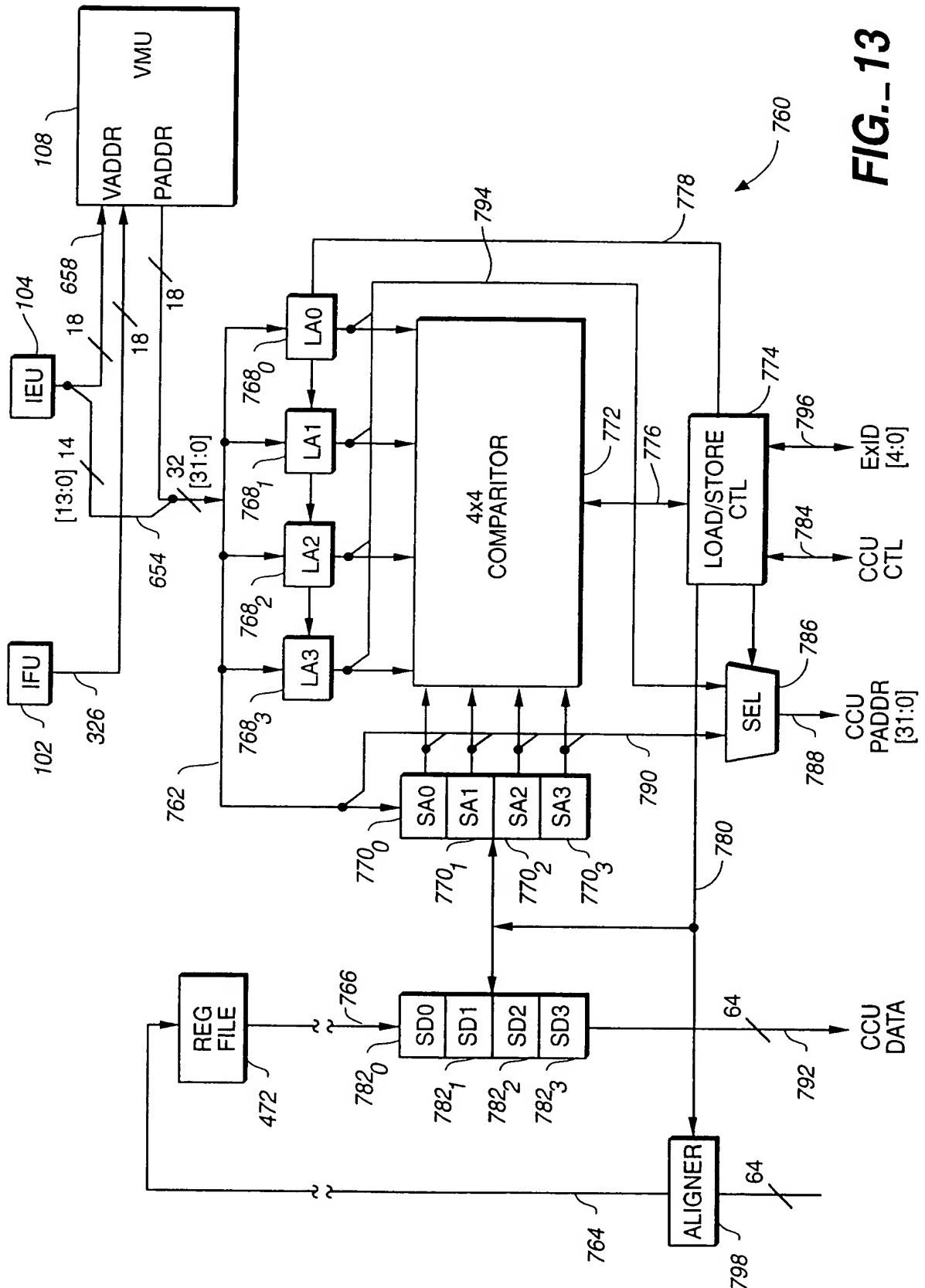


FIG. 13

Replacement Sheet

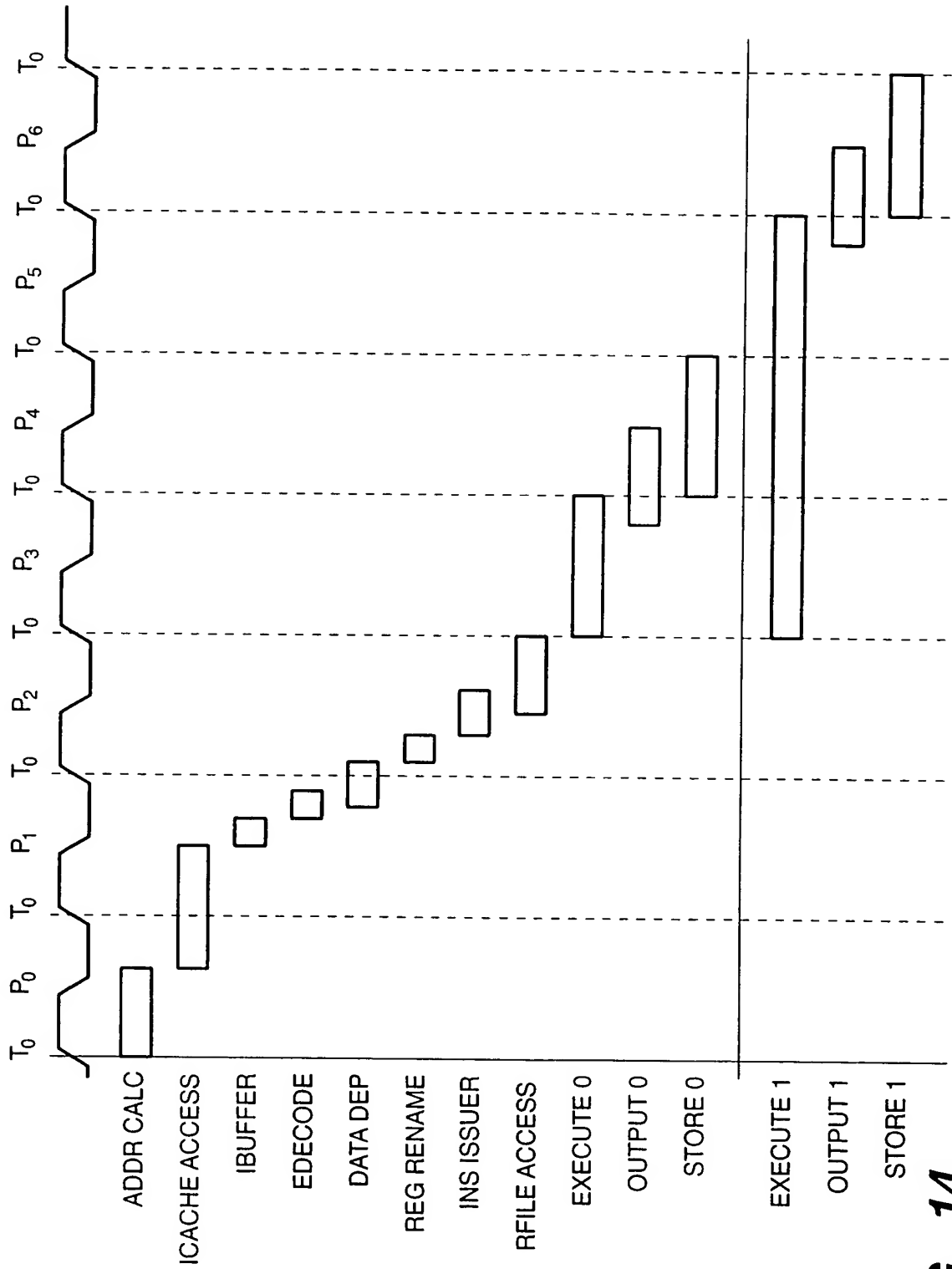
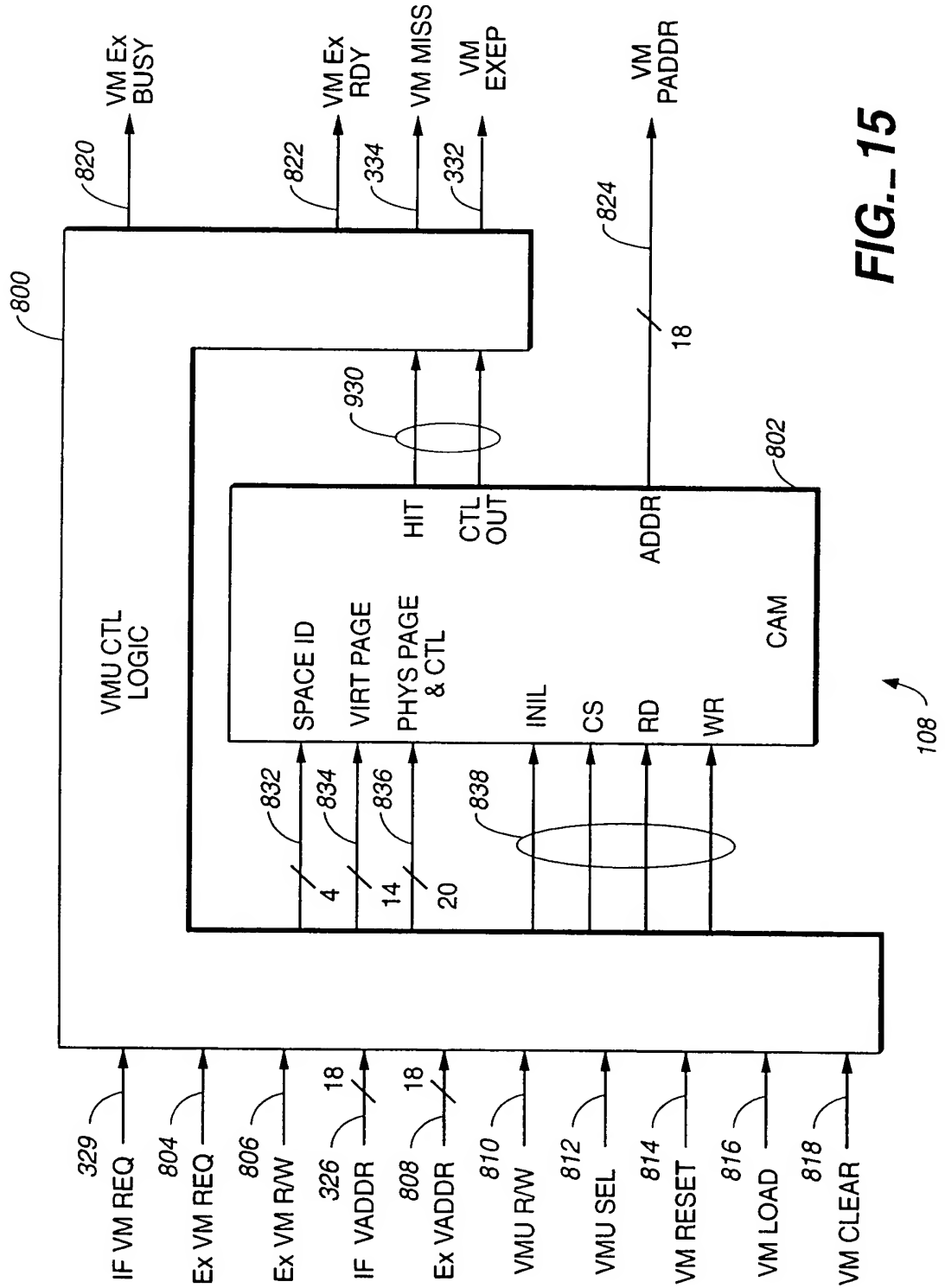


FIG. 14



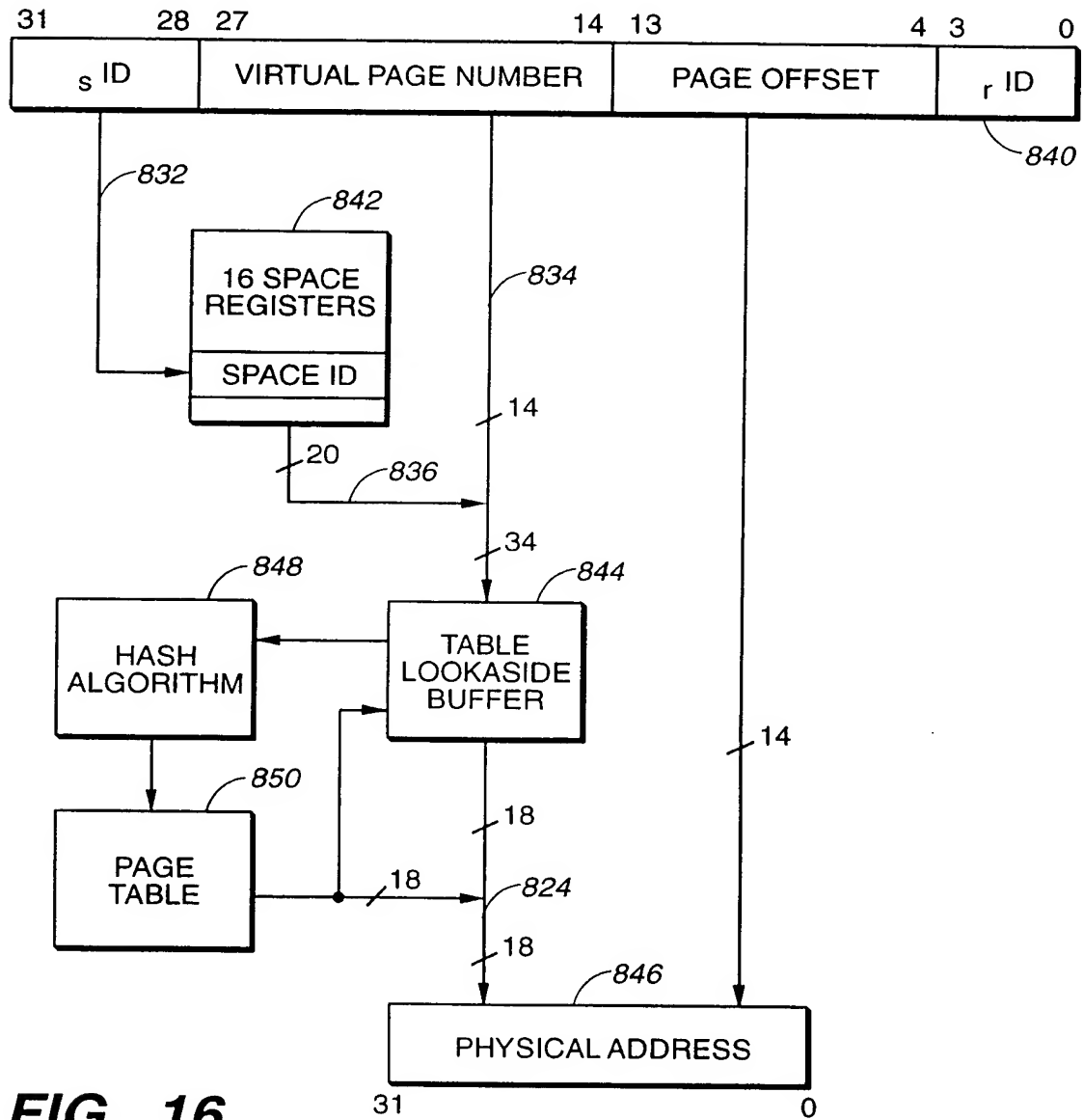


FIG. 16